A Combined Fault Detection and Discrimination Strategy for Resource-Sensitive Platforms

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Abstract. This paper presents a combined fault detection and discrimination strategy for CMOS logic incorporating active resource mitigation and monitoring. The approach is demonstrated for a NOR gate using a dual redundant gate design with selective mitigation and analogue or digital detection. The potential benefits of the approach are discussed with respect to resource awareness and management within fine-grained logic.

Keywords: Self-repair, fault detection, redundancy.

1 Introduction

Fault detection and mitigation within CMOS logic structures is a long-standing challenge that is seeing new a emphasis for nanoscale and printable electronics. The possibility for intrinsic resource awareness and management without obfuscating management at higher design levels is an attractive proposition but requires new gate and transistor level strategies. This paper presents ongoing work into a combined fine-grained redundancy and active mitigation approach with minimal resource overhead that enables selective fault detection, masking and discrimination close to the point of fault manifestation.

1.1 Existing Methods

On-line fault strategies have been discussed at length for future nanoscale electronics where massive redundancy concepts become feasible [1]. However, resource-sensitive platforms typically involve more conservative duplicate gate and/or interconnect structures combined with majority signal generation in order to mask faults and prevent their manifestation at critical outputs. Practical examples involving triple and quad redundancy are illustrated in Fig. 1a-b. Combined logic interleaving and quad-transistor structures have also been investigated [2]. While the use of regular cell structures is attractive, typical methods incur between 3–8 times resource overhead and do not achieve fault detection or discrimination. It could be argued that fault detection triggers may be generated within quad-transistor majority logic but determination of the specific fault location and its
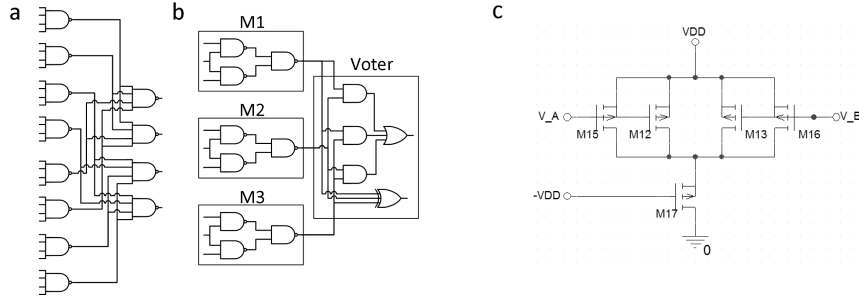
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Fig. 1. Traditional fault-tolerant designs. a) Quadded logic. b) Triple-modular redundancy with voter. c) pseudo-CMOS with redundancy.

type becomes abstracted by the internal process of converting critical faults to sub-critical faults.

Fine-grained fault tolerant strategies are beginning to feature in future nano-scale CMOS logic design with the principal aim of combating manufacturing defects. This includes psueo-CMOS redundancy, a simple example of which is illustrated in Fig. 1c. Another approach is reported in [3] wherein defects present in either N-type or P-type networks invokes switched active pull up or pull-down loads. In this case, however, defect detection is not part of the repair method and instead would be provided by additional built-in self-test (BIST) logic and possibly external test equipment. Hard-fault mitigation approaches have been proposed that are based on active switching matrices [4]. However, self-detection is once again not included as a part of the strategy.

Field-programmable gate arrays (FPGA) provide flexible platforms featuring configurable cellular architectures that support full or partial configuration. Since their total resource utilisation rarely approaches 100%, there are opportunities to provision redundant resources for fault mitigation. Even so, it is not yet clear how spare resources may be reallocated to support online fault detection and discrimination without resorting to external supervisory hardware/software as typified in [5]. While solutions based on custom programmable architectures have been proposed that aim to address this limitationby enabling dynamic resource allocation [6], fault detection is still achieved through data error detection and correction (EDC) hardware that is abstracted from the hardware fault.

2   Proposed Method

The proposed strategy relies upon an alternative method referred to here as *Stuck-At Fault Resilient* (SAFR) design, wherein fixed dual redundancy is combined with a fault triggering mechanism [7]. An example logic NAND gate implemented by the SAFR approach in comparison to the standard NAND gate design is shown in Fig. 2, where dual redundancy is employed within the P- and N-type networks. This is in contrast to quad redundant strategies (Fig. 2c).
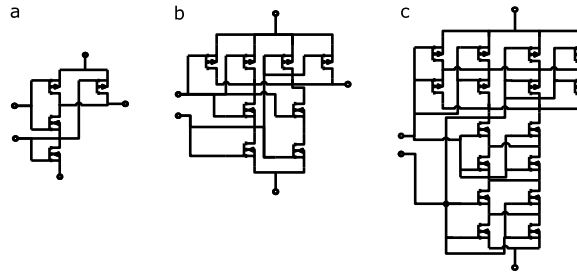
Fig. 2. Stuck-at fault resilient design. a) traditional NAND. b) proposed design. c) full quad-transistor design.

2.1   Detection Strategy

The dual redundancy strategy permits masking of any single stuck-off fault and selective fault triggers for stuck-on faults depending upon the state of the inputs. Of particular note is the fact that fault discrimination is not retained when higher redundancy factors are used i.e., triple- and quad-transistors. Hence, a resource trade-off between fault masking capacity and fault identification is present in this approach.

2.2   Discrimination and Mitigation

Selective fault masking allows for the detection of stuck-on faults considered to be critical due to potential high current flow between VDD and GND. Examination of the gate output response under fault condition, summarised in Table 1, shows that at there is at least one input combination that generates current flow between VDD and VSS for every single stuck-on fault. This may be exploited to achieve discrimination of fault type by monitoring current imbalance in the CMOS network or else periodic exercising of the gate inputs via digital test. The P- and N-networks are combined with the switching network for a NOR gate implementation are shown in Fig. 3, which includes weak active pull-up/down loads typically used for defect repair [3], but which are used here for selective online fault discrimination.

3   Resource Awareness and Management

Resource considerations will be important for emerging printable and nanoscale electronics due to their differing densities and scope for building redundancy structures based upon multi-gate and/or sub-gate nano-structures. Resource management extending to the fine-grained levels should be explored for both defect tolerance and hard-fault mitigation. Combining the above approach with weak active pull-up/down loads creates an efficient active mitigation mechanism that, when further combined with dual redundancy within the P- and

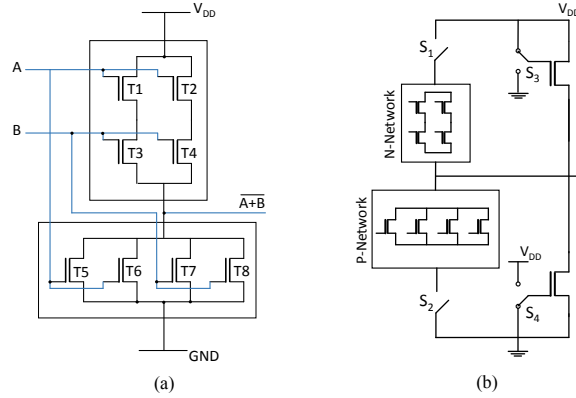4   A Combined Fault Detection and Discrimination Strategy

(a)   (b)

Fig. 3. Gate design strategy. (a) Example of redundancy scheme for NOR gate employing P- and N-type networks. (b) Potential implementation for active fault mitigation according to [3].

Table 1. Stuck-High Fault Response of CMOS Network

Input	Stuck-on fault location[a]							
AB	T1	T2	T3	T4	T5	T6	T7	T8
00	1	1	1	1	X	X	X	X
01	0	0	X	X	0	0	0	0
10	X	X	0	0	0	0	0	0
11	0	0	0	0	0	0	0	0

[a] Output error denoted by 'X'

N-networks, creates further resource awareness opportunities in the presence of faults. Once a fault has been detected, partial isolation proceeds by switching to pseudo-NMOS or PMOS mode wherein the nature of the fault may be further characterised. For example, assuming a stuck-at high fault occurring within the P-network (Transistors T1-T4 in Fig. 3a), the location of the fault is not known *a-priori*. The circuit may first be switched to pseudo-NMOS mode (setting switches S1 and S3 in Fig. 3b) and, due to the complimentary nature of the design, a second analogue/digital test will would reveal the same fault behaviour summarised in Table 1. However, depending on the value of the weak pull-down resistance of transistor T9, the digital test may pass without error and the adapted circuit may continue to be used in a degraded state. Alternatively, the circuit may be switched into pseudo-PMOS mode (switches S2 and S4) whereupon the error no longer persists. Hence the state of the P- and N-networks may be individually ascertained. The reverse situation of a fault occurring within the N-network would proceed in identical fashion as described above. At all times stuck-at low fault events are intrinsically masked.

An further extension of resource awareness concerns continual resource monitoring in the presence of intermittent faults. For the above case of the pseudo-PMOS configuration being activated in response to a stuck-high fault within the P-network, a further option would be to periodically switch to the pseudo-NMOS configuration and check the P-network response to determine whether the fault persists. This serves two functions: first, intermittent faults may be handled in a graceful manner and with specific knowledge of their locality. Second, disappearance of the fault allows for restoration of the full CMOS network and non-degraded performance.

4   Conclusions

Fault detection and discrimination remains a fundamental challenge in resource management for integrated fault mitigation. The proposed dual redundancy SAFR method achieves a combination of fault discrimination between stuck-high/stuck-low fault events and selective masking, thus reserving active mitigation for stuck-high faults. Fine-grained resource mitigation proceeds by combining redundancy with weak pull-up/down networks. Ongoing work is investigating further logic gate configurations and functional logic built from such gates.

Acknowledgement

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